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EXAMINER	
THOMAS, SHANE M	
ART UNIT	PAPER NUMBER
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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,564	LANDIN ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 24-34* is/are rejected.

7)☒ Claim(s) *21-23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *7/15/04 & 7/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the application filed 4/9/2004. Claims 1-34 are presented for examination and are currently pending.

In the response to this Office action, the Examiner politely requests that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line numbers in the specification and/or drawing figure(s). This will assist the Examiner in prosecuting this application.

Excerpts from all prior art references cited in this Office action shall use the shorthand notation of [column # / lines A-B] or paragraph number (¶) to denote the location of a specific citation. For example, a citation present on column 2, lines 1-6, of a reference shall herein be denoted as "[2/1-6]."

Priority

Domestic priority under 35 U.S.C. 119(e) to provisional case 60/462,010 has been acknowledged.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 4-14 and 30-34 are objected to because of the following informalities:

As per claim 4, the term --*the* read-to-own transaction-- should be amended to --a read-to-own transaction-- since the term has not been previously defined in the claims.

As per claim 13, the term --the address network-- should be amended to --the *additional* address network-- as the limitations of the claim pertain to the --additional node--.

As per claim 30, line 12 should be amended to read :

"coherency unit in response to an address packet on the address network,".

As per claim 34, the --include-- on line 2 should be amended to --includes--.

Claims 3-12,14, and 31-33 are objected to as being dependent upon an objected to base claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 15 and 16 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

The test for enablement is set forth as stated in MPEP §2164.01:

> Accordingly, even though the statute does not use the term "undue experimentation," it has been interpreted to require that the claimed invention be enabled so that any person skilled in the art can make and use the invention without undue experimentation. *In re Wands, 858 F.2d at 737, 8 USPQ2d at1404 (Fed. Cir. 1988).*

When considering the factors for determining whether there is sufficient undue experimentation evidence the breadth of the claims, nature of the invention, the direction provided by the inventor and the quantity of experimentation needed to make or use the invention based on the content of the disclosure, were all considered in light of the claims and Applicant's specification. Further, a search of the prior art was conducted as well in an attempt to ascertain whether such limitation of claims 15 and 16 would have been apparent to one of ordinary skill; the search did not reveal a clear, standard definition to the properties claimed.

As per claims 15 and 16, it is not readily apparent what the Applicant is claiming as the terms --ordered broadcasts property-- and --synchronized broadcasts property-- are not defined within Applicant's specification as originally filed. The specification mentions a --Synchronized Network Property-- (page 48, ¶142), a --Synchronized Multicasts Property-- (page 49, ¶143), and a --Network Convergence Property-- (page 51, ¶147), but neither of the claimed --properties--. Because the terms are not properly defined in the Applicant's specification and are not terms of art, the Examiner is unable to interpret the intended meaning of the limitations of claims 15 and 16.

Further regarding claim 15, the claimed term, while not a term of art, may elicit multiple meanings to one of ordinary skill in the art and does not necessarily imply one of the --properties-- defined in Applicant's specification. One example could have defined an "ordered broadcast" to be a group of requests or messages that are sent from one node to another

node or nodes such that the ordering of the messages was a logical order as seen by the sender node. Another such example could have defined "ordered broadcast" to be a group of messages that are received at the receiving node that are send from one or more other nodes in an arbitrary order and logically "ordered" by the receiving node. As a result of insufficient disclosure needed to make and use the invention as claimed by Applicant, experimentation needed to practice the invention is undue.

Further regarding claim 16, the --synchronized access priority-- claimed could not have been construed by one of ordinary skill in the art to be one of the --properties-- mentioned above in Applicant's specification. Specifically, the scope of the term --multicast-- of --synchronized multicasts property-- is not synonymous with the term --broadcast-- of --synchronized broadcasts property-- as stated in *IEEE 100 - The Authoritative Dictionary of IEEE Standards Terms* (refer to pages 121 and 712. As a result of insufficient disclosure needed to make and use the invention as claimed by Applicant, experimentation needed to practice the invention is undue.

Applicant is reminded of 37 C.F.R. 1.75 (d)(1) which states that the claim or claims must conform to the invention as set forth in the remainder of the specification and the terms and phrases used in the claims must find clear support or antecedent basis in the description so that the meaning of the terms in the claims may be ascertainable by reference to the description. (See 1.58(a).)

Nonetheless, for the purposes of examination, the Examiner has considered the terms using a broadest reasonable interpretation in light of the specification, as further discussed in the rejections that follow.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4-14, rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 4, it is not clear whether the term --*said corresponding* data packet-- is referring to the --data packet-- of parent claim 2 or to a different data packet, as the term --*said corresponding* data packet-- lacks antecedent basis. For the purposes of expedited examination, the Examiner has interpreted the term to be the data packet as defined in claim 2.

As per claim 5, a typographical error appears in line 2; therefore, it is not clear whether --*the* processing subsystem-- (previously defined in claim 1) receives a corresponding address packet or whether --a processing subsystem-- (e.g. any processing subsystem) receives a corresponding address packet. For the purposes of expedited examination, the Examiner has interpreted the term to be --the processing subsystem--.

Claims 6-14 are rejected as being dependent upon a rejected base claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1,2,15-20, 24,25, and 27, are rejected under 35 U.S.C. 102(b) as being anticipated by Singhal et al. (U.S. Patent No. 5,978,874).

As per claims 1, Singhal teaches:

(1) figure 2 - a node 50N including a processing subsystem 160N and an interface (combination of 140 and 180) coupled by an address network (dashed lines connecting the elements 150N-170N coupled to the address controller 180 and extending to the address bus/state lines 60 of the omnibus 30) and a data network (solid lines connecting data buffer 140 to the elements 150N-170N and extending through to the data bus lines 70 of the omnibus 30);

(2) an additional node (figure 1 shows a plurality of identical nodes 50, depicted in figure 2 in detail) including an additional processing subsystem 160-1 (i.e. the processor unit of node

50-1) and an additional interface (combination of elements 140 and 180 of node 50-1) coupled by an additional address network (defined above) and a data network (defined above);

(3) an inter-node network 30 configured to convey communications between the node and the additional node (refer to figure 1), wherein the interface and the additional interface are coupled (via the interconnect by their respective line-bundles 40-N) to send and receive communications on the inter-node network 30 - [6/49-51] and [12/53-61];

(4) wherein as part of a coherency transaction involving a coherency unit (e.g. a cache line) cached by the processing subsystem, the processing subsystem is configured to transition an access right to the coherency unit (e.g. the ability to write the cache line - [28/3-30]) and to transition an ownership responsibility for the coherency unit [14/54-56], wherein the processing subsystem transitions the access right at a different time than the processing subsystem transitions the ownership responsibility - ownership transitions immediately after a Read-to-Own transaction is issued [14/54-56] and access right is transitioned when a data packet is received [28/10-11].

As per claim 2, the access right to the coherency unit (cache line) cached by the processing subsystem transitions in response to the professing subsystem receiving a data packet via the data network (as defined above) - [28/3-11].

As per claim 15, the address network of Singhal (defined supra) implements an ordered broadcasts property - [29/66 - 30/5].

As per claim 16, the address network and the data network of Singhal implement a synchronized broadcast property as the nodes 50 are synchronized for requests via the Arbitration Unit 186 (figure 3) - [20/46-63].

As per claim 17, the access right to the coherency unit cached by the processing subsystem (in this case the coherency unit is buffered in a bcopy buffer or a streaming I/O buffer as will be described) transitions in response to the processing subsystem receiving a data packet via the data network [28/10-11], wherein the data packet is provided to the processing subsystem as part of a write stream transaction [16/49 - 17/7] initiated by the processing subsystem. Here, the initiating processing subsystem is the "initiator" and the processing subsystem considered to be the "home node" of the requested data is the "responder."

As per claim 18, the data packet is an encoded acknowledgement (data packet sent from the responder is encoded to only contain the DataID when ready to accept the data - [16/66 - 17/4]) that excludes data (only the DataID is sent as discussed) corresponding to the coherency unit (e.g. cache line).

As per claim 19, the rejection for the limitations of lines 1-10 follows the rejection set forth in claim 1. Singhal further teaches wherein the processing subsystem is configured to transition an access right to a coherency unit (e.g. cache line) in response to a data packet on the data network [28/3-30] and to transition an ownership responsibility for the coherency unit in response to an address packet on the address network [14/53-56].

As per claim 20, the address packet and the data packet are part of a transaction (Read-to-Own) initiated by the processing subsystem - [14/19-67], wherein the transaction also includes an additional address packet (local address packet once received over the omnibus 30 - [14/32-34]) sent on the additional address network (the responder's (e.g. cache line owner) portion of its address bus (portion of line buses 40) and at least one message sent on the inter-node network 30

- the asserting of the Owned signal and the fulfilling of a response from the owner processor [14/40-42].

As per claim 24, the transaction is a read-to-own transaction [14/17-67], wherein the processing subsystem is configured to initiate the read-to-own transaction by sending a read-to-own packet on the address network [12/47 - 13/5].

As per claim 25, wherein no memory subsystem (i.e. memory 150) included in the node (i.e. the requesting node) maps the coherency unit (i.e. the memory line is mapped to another node or device 50) - [14/28-39] and [22/1-19], wherein in response to the read-to-own packet on the address network, the interface (elements 140 and 180) is configured to send a read-to-own message to the additional interface in the additional node (messages sent via the omnibus 30 in a broadcast method - [12/47-62].

As per claim 27, the address network conveys the address packet in broadcast mode [7/37-40].

Claims 1-14,19,26, and 28-34, are rejected under 35 U.S.C. 102(e) as being anticipated by Gharachorloo et al. (U.S. Patent Application Publication No. 2002/0124144).

As per claim 1, Gharachorloo teaches:

(1) a node 102 in figure 1 which includes a processing subsystem (combination of CPU 106 and associated caches 108 and 110) and an interface (combination of elements 122,124,136,130,12, and 128) coupled by an address network and a data network (112 as well as interconnects that couple the components of the interface together), since the interface is capable of sending and receiving both data and address requests/responses (¶158);

(2) an additional node 102, 104 including an additional processing subsystem (106,108,110) and an additional interface (as define above) coupled by an additional address network and an additional data network (as defined above) - ¶49 teaches multiple nodes are components of the system of figure 1;

(3) an inter-node network 134 configured to convey communications between the node and the additional node, wherein the interface and the additional interface are coupled to send and receive communications on the inter-node network - ¶50;

(4) wherein as part of a coherency transaction involving a coherency unit (e.g. a cache line) cached by the processing subsystem, the processing subsystem is configured to transition an access right to the coherency unit (e.g. the ability to write the cache line where the cache line becomes an Active transaction - ¶170) and to transition an ownership responsibility for the coherency unit - ¶177, wherein the processing subsystem transitions the access right at a different time than the processing subsystem transitions the ownership responsibility - ownership transitions when the Home Node for the coherency unit send a read-exclusive forward message to the previous owner node -¶177 and access right is transitioned when the RPE 124 of the interface forwards (1) the memory line of the coherency unit (¶181) and (2) activates the memory transaction (¶170), which takes place when all invalidation acknowledgements have been received - ¶183.

As per claim 2, the access right to the coherency unit cache by the processing subsystem transitions in response to the processing subsystem receiving a data packet via the data network- ¶180-183. In the case when all invalidation acknowledgements have been received before the requested memory line (¶180), the Examiner is considering the forwarding of the requested

memory line (coherency unit) from the RPE 124 to the requesting processing subsystem 106 to be the --data packet--; and in the case when the memory line is received and forwarded to the processing subsystem 106 before all acknowledgements have been received, the Examiner is considering the additional message sent from the RPE 124, that results in the TSRF entry 210 corresponding to the memory line becoming Active, to the processing subsystem as the --data packet--.

As per claim 3, the interface (specifically, the RPE 124) in the node is configured to delay providing --data corresponding to the coherency unit-- on the data network (switch 112) until the interface has received an indication that shared copies of the coherency unit in the additional node (in this case either the home node or owner node) have been invalidated - ¶182. Here, the Examiner is considering the "additional message" sent by the RPE 124 (¶182) to the requesting processor 106 to be --data associated with the coherency unit-- as this message contains an affirmation that the coherency unit in the additional node has been invalidated. Once received the TSRF entry associated with the transactions can be made active in order to be utilized by the requesting processor - ¶183.

As per claim 4, the corresponding data packet received by the processing subsystem is conveyed on the data network by the interface 112 as part of a read-to-own transaction (read-exclusive transaction, as the requestor of the read-exclusive transaction becomes the owner) - ¶¶177-183. The rejection of the remainder of the claim (lines 3-5) follows the rejection for claim 3, above.

As per claim 5, the ownership responsibility corresponding to the coherency unit (e.g. memory line) cached by the processing subsystem transitions (i.e. loses ownership) in response

to the processing subsystem receiving a corresponding address packet (which corresponds to a read-exclusive request sent by a requesting node) via the address network (specifically switch 112 that receives an invalidation request that uses the address packet to forward the invalidation to the processing subsystem - ¶171). As another node has requested ownership for the memory line, the directory associated with the home node containing this processing subsystem is updated to indicate the requesting node's ownership when the invalidation (e.g. corresponding address packet) is sent on the address network - ¶172.

As per claims 6 and 31, the address packet is a read-exclusive packet as defined above. Applicant's originally filed specification stated on page 39 (¶121) that a read-to-own packet when a cache miss occurs at a requesting node and the requesting processing subsystem request write permission to the cache line. The read-exclusive packet of Gharachorloo performs the same functionality of a read-to-own packet as a requesting processor in that a request is made for an exclusive copy of the memory line in order for the requesting processor to modify the memory line (¶170). If the processor does not already have an updated copy of the memory line, a copy of the line is provided with the response (¶181).

As per claim 7, the read-to-own transaction (read-exclusive request) is initiated by the processing subsystem conveying the address packet on the address network - step 1200 of figure 12A and ¶170.

As per claim 8, the interface (specifically the RPE 124) is configured to forward a read-to-own message corresponding to the address packet (i.e. the read-exclusive address request) to the additional interface via the inter-node network 134 in response to receiving the address

packet - ¶170. The received request is forwarded to the home node, where additional processing takes place as taught in ¶170.

As per claim 9, the coherency unit is not mapped by any memory subsystem included in the node and wherein the additional node is a home node for the coherency unit. This can be seen as the request must be forwarded to the home node for the memory line in order to obtain the data ¶¶171-172.

As per claim 10, the Examiner is considering the intra-chip switch interfaces (herein "ISI") 156 of the processing subsystems (refer to figure 3) to be part of the address network as the ISI is responsible for communication and message passing between switch 112 and the processor subsystem (106,108, and 110) - ¶61. In response to the address packet portion (e.g. the read-exclusive request's inherent address portion, as a receiving node must know what data is being requested in order to fulfill the read-exclusive request thereby making the address packet an inherent portion of a read-exclusive transaction) of a read-exclusive request being sent from the processing subsystem (¶170 and figure 12A, step 1200) and received via the output queue 162 of the address network (figure 3 and ¶61), a memory subsystem (output queue 162) included in the node is configured to send a data packet (e.g. a packet encoded as a read-exclusive request that contains the requested memory address as well as an indication that the processor 106 requests exclusive access as opposed to read/share access (¶159), as the processor 106 is responsible for initializing such a request - ¶170) indicating the read-to-own (read-exclusive) transaction to the interface (specifically, the switch 112 portion of the interface as defined supra), wherein the interface (specifically, the RPE 124) is configured to forward a read-to-own message

on the inter-node network 134 (i.e. to the home node for the memory line) in response to receiving the data packet indicating the read-to-own transaction (¶170).

As per claim 11, the additional interface (in this case the home node's interface) is configured to receive the read-exclusive message via the inter-not network 134 (¶171) and to responsively send an invalidating address packet on the additional address network (as defined supra) (¶171 - where the invalidating address packet is sent to the L2 cache to invalidate the memory line in the caches of the home node). The limitation of lines 4-6 are not specifically taught by Gharachorloo as the Examiner has shown that an access right to a memory line is obtained after gaining ownership; therefore, it can be seen that a processing subsystem may never have an access right to not ownership responsibility for a memory line. Nonetheless, as this limitation is drafted in the alternative, and therefore may not necessarily occur with regards to Applicant's claimed invention, the limitation is met by Gharachorloo.

As per claim 12, wherein in response to receiving the invalidating address packet on the additional address network, the additional interface is configured to send via the inter-node network 134 a message indicating that copies of the coherency unit (memory line) in the additional node (i.e. the home node) have been invalidated to the interface (¶172). The reply sent from the home node to the requesting node, which includes the memory line, includes the number of invalidation acknowledgements that are outstanding from other nodes. This message thereby indicated that the copies of the data cached in the home node have been invalidated.

As per claim 13, the additional interface is configured to send an additional address packet on the address network (e.g. the address packet used to invalidate the cache of the processor caches 108,110), wherein if the additional processing system has an ownership

responsibility associated with the coherency unit, the additional processing system is configured to transition the ownership responsibility (e.g. invalidate its copy) upon receiving the additional address packet (¶171). Such a transition is reflected in the directory 180 which contains ownership responsibilities for all processing subsystems of a given node - see ¶66 and ¶75.

As per claim 14, wherein the additional processing system is configured to send a data packet corresponding to the coherency unit to the additional interface in response to receiving the additional address packet (e.g. the up-to-date memory line is sent from the owner node to the requesting node - ¶178), wherein the additional processing subsystem is configured to transition an access right (i.e. invalidate its cached copy of the requested data) associated with the coherency unit in response to sending the data packet corresponding to the coherency unit - ¶178.

As per claim 19, the rejection of lines 1-10 follows the rejection of claim 1, lines 1-10 set forth above. Gharachorloo also teaches:

(1) [note in this case the processing subsystem is considered as being contained on a requesting node that issues a read-exclusive request for a memory line] wherein the processing subsystem is configured to transition an access right (ability to write or modify the requested data) to a coherency unit (memory line) in response to a data packet (message from RPE 124 that all invalidation acknowledgements have been received that is sent to the requesting processor 106 - ¶182) on the data network (message sent via the switch 112 portion of the data network, as defined supra); and

(2) [note in this case the processing subsystem is considered as being contained on a home node that has received a read-exclusive request for a memory line from a requesting node] to transition an ownership (e.g. lose ownership rights) responsibility for the coherency unit in

response to an address packet on the address network (e.g. receiving a read-exclusive request for a memory line) - ¶172, which teaches that the home node indicates in the directory 180 that the requesting node is now the owner of the memory line. It is inherent that the read-exclusive request packet contain an address packet portion in order for the home node to retrieve and send the correct requested data when receiving the read-exclusive request.

As per claim 26, Gharachorloo teaches the address network (specifically the switch 112) is configured to convey the address packet (e.g. the address portion of the read-exclusive request packet) from a directory (e.g. a Dtag array) to the processing subsystem (i.e. when the address is used to invalidate data cached locally that is associated with a received read-exclusive request) in a point-to-point mode (this can be seen since the invalidation is only sent to those processing subsystems (e.g. combination 106,108, and 110) which contain the data corresponding to the read-exclusive request via switch 112) - ¶171. The Dtag array is used to locate which processor caches contain the data to be invalidated from the received address packet, and the L2 cache executes a point-to-point invalidation request using the address packet (i.e. the address packet inherently must be sent as it contains the address of the associated memory line to be invalidated) to only those caches 108,110 that contain the associated data.

As per claim 28, the rejection of lines 1-10 follows the rejection for claim 1 as set forth above. Gharachorloo also teaches:

(1) wherein the processing system (for this limitation considered to be in the home node which receives a read-exclusive request from another node) is configured to transition an access right (e.g. lose the ability to write a requested cache line) to a coherency unit in response to sending a data packet (memory line) corresponding to the coherency unit on the data network

(¶172 shows that a memory line is sent from the processing system of the home node via the home node's data network, across the inter-node connection 134 to the requesting node); and

(2) [for this limitation the processing subsystem is considered to be located on a node requesting an exclusive copy (read-exclusive request)] wherein the interface within the node is configured to delay providing an additional data packet (e.g. an additional message sent from the RPE 124 of the interface to the requesting processing subsystem 106 which indicates that all invalidation acknowledgements have been received - ¶182) corresponding to an additional coherency unit (i.e. a memory line that is being requested as opposed to the memory line being forwarded to another node, discussed above in the previous limitation) on the data network (switch 112, part of the interface and defined supra, links the RPE 124 to the requesting processing subsystem - figure 1) until the interface receives via the inter-node network 134 an indication (e.g. invalidation acknowledgement) that a shared copy of the additional coherency unit in the additional node (e.g. the home node for the requested additional coherency unit) has been invalidated - ¶¶181-183.

As per claim 29, the rejection of lines 1-6 follows the rejections for lines 1-10 of claim 1 above, and the rejection of lines 7-9 follow the rejection for claim 3, wherein the --client devices-- are considered to the --processing subsystems--. The rejection of lines 10-15 follows the rejection of lines 10-14 of claim 19, wherein the --active device-- a processor cluster (e.g. combination of CPU 106 and corresponding caches 108 and 110) that is affected by the immediate memory request. Specifically, the limitation of lines 10-12 is being considered to occur to be when the active device requests a memory line and is therefore contained on a requesting node, and the limitation of lines 13-15 is being considered to occur when the active

device is contained on a home node, where it locally caches a copy of the requested memory line. Refer to ¶172 and ¶¶181-183.

As per claim 30, Gharachorloo teaches:

(1) a processing subsystem (combination of CPU 106 and associated caches 108 and 110) in a node 102 requesting an access right to a coherency unit (memory line) by conveying an address packet (as discussed above, a read-exclusive request inherently contains and address packet portion to convey the address of the requested memory line) on an address network (i.e. portion the address network coupling the requesting CPU 106 to the HPE that sends out the request to the home node - ¶172) included in the node 102;

(2) an interface (combination of elements 122,124,136,130,12, and 128) in to the node 102 delaying providing a data packet (additional message sent from the RPE 124 to the requesting processor 106 upon receiving a last invalidation acknowledgement - ¶182) corresponding to a coherency unit on a data network (i.e. the data switch 112 that couples the processors 106 and the RPE 124) included in the node 102 (figure 1) until the interface receives an indication (e.g. invalidation acknowledgement) that shared copies of the coherency unit in an additional node 102,104 have been invalidated (¶¶181-182), wherein the additional node includes a different address network and different data network (figure 1 shows the internal organization of node0, and node1 is a similar processing node and therefore would have its own internal address and data network - ¶49);

(3) [note that for this limitation the Examiner is considering the case when the processing subsystem requests the memory line and therefore is contained on the requesting node] the processing subsystem gaining the access right to the coherency unit in response to the data

packet on the data network - ¶¶182-183, as the additional message sent from the RPE 124, signifying that all invalidations are complete, "Activates" the memory transaction (e.g. gaining the access right);

(4) [note for this limitation the Examiner is considering the case when the processing subsystem is contained on a home node that receives a request for a memory line from another node and relinquishes ownership of a memory line] the processing subsystem transitioning ownership responsibility (e.g. ownership switched to the to the requesting node - ¶172) for the coherency unit in response to an address packet on the address network (e.g. a read-exclusive request's associated address packet - ¶171, which changes the ownership in the directory 180 - ¶172) wherein the gaining occurs at a different time than the transitioning (since the gaining occurs when the home node requests a read-exclusive requests and verifies that all other copies have been invalidated and the transitioning may occur later when the home node loses ownership when a remote node (such as Node1) issues a read-exclusive request for the same memory line that the node previously owned and gained access rights to, it can be seen that the gaining and transitioning may occur "at different times."

As per claim 32, Gharachorloo further teaches:

(1) the interface (specifically the RPE 124 portion of the interface) [of the requesting node] sending a read-to-own message (e.g. read-exclusive request) to an additional interface (specifically, the HPE 122 of the home node) in the additional node (e.g. the home node for the requested data line) in response to said requesting (¶¶170-171);

(2) the additional interface sending an invalidation packet on the different address network (specifically, to the L1 and L2 caches via the switch 112) included in the additional node 102,104 in response to receiving the read-to-own message (¶171); and

(3) an additional processing subsystem in the additional node transitioning an access right to the coherency unit to an invalid access right in response to receiving the invalidating packet on the different address network (¶172 - the directory 180 corresponding to the additional processing subsystem (and for that matter all processing subsystem of the specific node) is updated to indicate that the requesting processor exclusively owns the line and therefore access writes must be obtained therefrom).

As per claim 33, the additional interface (corresponding to the home node) provides an indication (e.g. invalidation acknowledgement) that the shared copy of the coherency unit in the additional node has been invalidated to the interface (RPE 124 of the requesting node) in response to receiving the invalidating packet on the different address network - ¶172.

As per claim 34, the rejection for lines 1-11 follows the rejection of claim 1, lines 1-9; the rejection for lines 12-15 follows the rejection of claim 3; the rejection for lines 16-19 follows the rejection of claim 2, and the rejection for lines 20-22 follows the rejection of claim 19, lines 13-14.

Allowable Subject Matter

Claims 21-23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

As per claim 21, the prior art of record does not specifically teach or suggest, either alone or in combination, delaying the data packet until the interface receives an indication from the additional interface that shared copies of the cache line have been invalidated. Specifically, the prior art reference of Singhal teaches away from delaying requested data being sent to the requesting processing subsystem based on waiting for invalidation acknowledgements [28/66 - 29/20].

The prior art reference of Gharachorloo fails to specifically teach or suggest the limitations of claim 21. The address packet and the data packet, while both being part of a read-exclusive transaction, are not part of a transaction "initiated by the processing subsystem." The Examiner's rejection of base claim 19 states that the --address packet-- of Gharachorloo was interpreted as part of a read-exclusive transaction initiated from a different processing subsystem in another node. Because Gharachorloo fails to teach claim 20, the reference therefore fails to teach dependent claim 21.

Claims 22 and 23 are objected to as being dependent upon an objected to base claim.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Arimilli et al. (U.S. Patent Application Publication No. 2003/0009643) teaches the that cache line ownership transitions for a node at a different time than cache line access rights (¶¶119-120).

Cypher (U.S. Patent No. 9,928,519) and Cypher et al. (U.S. Patent No. 7,032,078) may be combined in a 35 U.S.C. §103(a) rejection to reject at least a portion of claims 1-34; however, in order to prevent an over-rejection of the claims, the §103(a) rejection has not been applied. Additionally, the Cypher and Cypher et al. references have a common assignee with the instant application and therefore, should the rejection be applied, would be eligible to be overcome by (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c); or (4) by showing that the reference is

disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M. Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M. Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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